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<u>L36</u>	L35 and ((reallocat\$3 or re-alloc\$3) adj5 portion adj5 cache)	1	<u>L36</u>
<u>L35</u>	((711/104  711/105  711/115  711/165  711/170  711/172  711/173  711/129  711/153  711/154  711/171 )!.CCLS. )	3596	<u>L35</u>

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<u>L34</u>	L32 and (cach\$3 adj3 director\$3)	3	<u>L34</u>
<u>L33</u>	L32 and (cache adj3 director\$3)	2	<u>L33</u>
<u>L32</u>	(5276832.pn.) or l29 or l28 or l24 or l23	90	<u>L32</u>
<u>L31</u>	5276832.pn. and remov\$	1	<u>L31</u>
<u>L30</u>	L29 and remov\$	2	<u>L30</u>
<u>L29</u>	5784548.pn.	2	<u>L29</u>
<u>L28</u>	(removabl\$5 adj3 cache)	30	<u>L28</u>
<u>L27</u>	(removabl\$5 adj3 dram)	4	<u>L27</u>
<u>L26</u>	l4 and (removabl\$5 adj3 dram)	1	<u>L26</u>

<u>L25</u>	L24 and (((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3))	0	<u>L25</u>
<u>L24</u>	6098132.pn. or 5943482.pn. or 6101322.pn.	6	<u>L24</u>
<u>L23</u>	l18 and (((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3))	52	<u>L23</u>
<u>L22</u>	l20 or L21	9	<u>L22</u>
<u>L21</u>	(((hot adj2 remov\$3)) with memor\$3)).ab,ti.	5	<u>L21</u>
<u>L20</u>	(((hot adj2 add\$3)) with memor\$3)).ab,ti.	4	<u>L20</u>
<u>L19</u>	20020069322.pn.	2	<u>L19</u>
<u>L18</u>	(((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3)).ab,ti.	52	<u>L18</u>
<u>L17</u>	(((plug adj3 play) or (hot adj2 swap\$5)) same memor\$3)).ab,ti.	89	<u>L17</u>
<u>L16</u>	(((plug adj3 play) or (hot adj2 swap\$5)) and memor\$3)).ab,ti.	144	<u>L16</u>
<u>L15</u>	L10 and (cach\$3 adj3 director\$3)	1	<u>L15</u>
<u>L14</u>	L12 and (cach\$3 adj3 director\$3)	4	<u>L14</u>
<u>L13</u>	L12 ahd (cach\$3 adj3 director\$3)	4133	<u>L13</u>
<u>L12</u>	(((plug adj3 play) or (hot adj2 swap\$5)) same cach\$3)	55	<u>L12</u>
<u>L11</u>	(((plug adj3 play) or (hot adj2 swap\$5)) adj3 memor\$3)	56	<u>L11</u>
<u>L10</u>	(((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3)	357	<u>L10</u>

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<u>L9</u>	L6 and (((plug adj3 play) or (hot adj2 swap\$5)) with memor\$3))	0	<u>L9</u>
<u>L8</u>	L6 and ((plug adj3 play) adj5 memor\$3)	0	<u>L8</u>
<u>L7</u>	L6 and ((hot adj2 swap\$5) adj5 memor\$3)	0	<u>L7</u>
<u>L6</u>	L4 and ss-dasd	0	<u>L6</u>
<u>L5</u>	L4 and ssdasd	0	<u>L5</u>
<u>L4</u>	l1 or l2 or L3	17282	<u>L4</u>
<u>L3</u>	((711/104  711/105  711/115  711/165  711/170  711/172  711/173 )!..CCLS. )	2469	<u>L3</u>
<u>L2</u>	((710\$)!..CCLS.)	14856	<u>L2</u>
<u>L1</u>	((713/100 )!..CCLS. )	590	<u>L1</u>

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System Sciences, 1997, Proceedings of the Thirtieth Hawaii

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Page(s): 168 -177 vol.5

[\[Abstract\]](#) [\[PDF Full-Text \(972 KB\)\]](#) **IEEE CNF****2 Multicast with cache (Mcache): an adaptive zero-delay video-on-demand service***Ramesh, S.; Injong Rhee; Guo, K.;*

INFOCOM 2001. Twentieth Annual Joint Conference of the IEEE Computer and Communications Societies. Proceedings. IEEE,

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[\[Abstract\]](#) [\[PDF Full-Text \(608 KB\)\]](#) **IEEE CNF****3 Role of download time as a key in Web cache management policies***Fonseca, N.L.S.; Oliveira, R.M.;*

Global Telecommunications Conference, 2001. GLOBECOM '01. IEEE,

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**4 Multicast with cache (Mcache): an adaptive zero-delay video-on-demand service**

*Ramesh, S.; Rhee, I.; Guo, K.;*

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**5 Reducing cache conflicts by partitioning and privatizing shared arrays**

*Zhiyuan Li;*

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**6 Coordinating simultaneous caching of file bundles from tertiary storage**

*Shoshani, A.; Sim, A.; Bernardo, L.M.; Nordberg, H.;*

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Page(s): 196 -206

[\[Abstract\]](#) [\[PDF Full-Text \(180 KB\)\]](#) **IEEE CNF**

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*Chau, S.N.; Reh, K.R.; Cox, B.; Barfield, J.N.; Lockhart, W.L.; McLlland, M.L.;*

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Page(s): 165 -176 vol.1

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### 2 Developing plug-and-play spacecraft systems: NASA Goddard Space Flight Center's (GSFC) Essential Services Node (ESN)

*Caffrey, R.; Shaw, H.; Wagner, L.;*

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Page(s): 2.1 -28-35 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(548 KB\)\]](#) **IEEE CNF**

### 3 The Windows NT kernel architecture

*Solomon, D.A.;*

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Page(s): 40 -47

[\[Abstract\]](#) [\[PDF Full-Text \(200 KB\)\]](#) **IEEE JNL**

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[\[Abstract\]](#) [\[PDF Full-Text \(52 KB\)\]](#) **IEEE CNF****2 Code transformations to improve memory parallelism***Pai, V.S.; Adve, S.;*

Microarchitecture, 1999. MICRO-32. Proceedings. 32nd Annual International Symposium on , 16-18 Nov. 1999

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[\[Abstract\]](#) [\[PDF Full-Text \(108 KB\)\]](#) **IEEE CNF****3 Assessment of gait parameter in hemiplegic patients by accelerometry***Sekine, M.; Abe, Y.; Sekimoto, M.; Higashi, Y.; Fujimoto, T.; Tamura, T.; Fukui, Y.;*

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Page(s): 1879 -1882 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(284 KB\)\]](#) **IEEE CNF**

**4 Development of a new wearable multi-channel sensing unit**

*Naemura, K.; Hosaka, H.; Iseki, H.; Itao, K.*

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Page(s): 3874 -3877 vol.4

[\[Abstract\]](#) [\[PDF Full-Text \(425 KB\)\]](#) **IEEE CNF**

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**5 An instrument with a DSP for monitoring human biological parameters**

*Buizza, A.; Coldani, G.; Danese, G.; Gandolfi, R.; Ghidetti, P.; Lombardi, R.*

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[\[Abstract\]](#) [\[PDF Full-Text \(328 KB\)\]](#) **IEEE CNF**

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**6 Portable acquisition system for measurements of pressures, temperatures and humidity in lower limb prosthesis**

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Page(s): 368 -371

[\[Abstract\]](#) [\[PDF Full-Text \(376 KB\)\]](#) **IEEE CNF**

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*Pai, V.S.; Ranganathan, P.; Abdel-Shafii, H.; Adve, S.*

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[\[Abstract\]](#) [\[PDF Full-Text \(492 KB\)\]](#) **IEEE JNL**

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**8 Data acquisition system for measurements in free moving subjects and its applications**

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Page(s): 878 -884

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Page(s): 8 -14

[\[Abstract\]](#) [\[PDF Full-Text \(216 KB\)\]](#) **IEEE CNF**

---

**15 Tracking performance of leakage LMS for chirped signals**  
*Ting, L.K.; Cowan, C.F.N.; Woods, R.F.; Cork, P.R.; Sprigings, C.J.;*  
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Page(s): 101 -108

[\[Abstract\]](#) [\[PDF Full-Text \(352 KB\)\]](#) **IEEE CNF**

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**16 Improving cluster IO performance with remote efficient access to distant device**  
*Cozette, O.; Randriamaro, C.;*  
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Page(s): 629 -635

[\[Abstract\]](#) [\[PDF Full-Text \(1137 KB\)\]](#) **IEEE CNF**

---

**17 Two-level hierarchical Z-Buffer for 3D graphics hardware**  
*Cheng-Hsien Chen; Chen-Yi Lee;*  
Circuits and Systems, 2002. ISCAS 2002. IEEE International Symposium on , Volume: 2 , 26-29 May 2002  
Page(s): II-253 -II-256 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(418 KB\)\]](#) **IEEE CNF**

---

**18 New results on array contraction [memory optimization]**  
*Darte, A.; Huard, G.;*  
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Page(s): 359 -370

[\[Abstract\]](#) [\[PDF Full-Text \(361 KB\)\]](#) **IEEE CNF**

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**19 A transistorless-current-mode static RAM architecture**  
*Levy, H.J.; Daniel, E.S.; McGill, T.C.;*  
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Page(s): 669 -672

---

[\[Abstract\]](#) [\[PDF Full-Text \(148 KB\)\]](#) **IEEE JNL**

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**20 Equilibrium characterization of dynamical neural networks for synthesis of associative memories**

*Sudharsanan, S.I.; Sundareshan, M.K.;*

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Page(s): 2744 -2749 vol.5

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**21 ASDM-a novel neural network model based on sparse distributed memory**

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Page(s): 771 -776 vol.1

---

[\[Abstract\]](#) [\[PDF Full-Text \(428 KB\)\]](#) **IEEE CNF**

---

**22 Vector quantization of contextual information for lossless image compression**

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Page(s): 390 -399

---

[\[Abstract\]](#) [\[PDF Full-Text \(452 KB\)\]](#) **IEEE CNF**

---

**23 Friendly and efficient message handling**

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Page(s): 121 -130 vol.1

---

[\[Abstract\]](#) [\[PDF Full-Text \(928 KB\)\]](#) **IEEE CNF**

---

**24 An efficient incremental algorithm for identifying consistent checkpoints**

*Loon-Been Chen; I-Chen Wu;*

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Page(s): 122 -129

[\[Abstract\]](#) [\[PDF Full-Text \(292 KB\)\]](#) **IEEE CNF**

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**25 A challenge over 100 Gbit/in<sup>2</sup> rewritable/removable MO storage**

*Itoh, A.;*

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Page(s): 86 -88

[\[Abstract\]](#) [\[PDF Full-Text \(144 KB\)\]](#) **IEEE CNF**

---

[1](#) [2](#) [\[Next\]](#)

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Parallel and Distributed Simulation, 2001. Proceedings. 15th Workshop on, 15-18 May 2001

Page(s): 56 -63

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Page(s): 978 -982

[\[Abstract\]](#) [\[PDF Full-Text \(310 KB\)\]](#) **IEEE CNF****28 Software quality classification modeling using the SPRINT decision tree algorithm***Khoshgoftaar, T.M.; Seliya, N.;*

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**29 A board system for high-speed image analysis and neural networks***Sackinger, E.; Graf, H.-P.;*

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Page(s): 214 -221

[\[Abstract\]](#) [\[PDF Full-Text \(1028 KB\)\]](#) **IEEE JNL****30 An efficient pipelined parallel architecture for blocking effect removal in HDTV***Jae-Wook Lee; Myung-Hoon Yang; Sungho Kang; Yoonsik Choe;*

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Page(s): 508 -512

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